IN THE CLAIMS:

Please amend claim 1 as follows:

1. (currently amended) A ~~M~~method of clocking an IP core during a debugging operation, characterized by switching from ~~the~~ a clock used for testing a design mapped onto an emulator to a clock oscillator or any free-running clock source.

2. (currently amended) The method of claim 1, wherein said switching is to said clock oscillator, which is provided on ~~the~~ an IP-Xpress board.

3. (currently amended) The method of claim 1 ~~or 2~~, wherein the clock used for testing the design ~~is a design clock used for testing~~ is either:

a) a clock sourced from the design mapped into the emulator

b) a clock sourced directly from the emulators clock generator circuits

c) a clock oscillator locally mounted on the IP-Xpress daughter board, or any free running clock source

4. (currently amended) The method of claim 1~~, 2 or 3~~, comprising the step of monitoring signals specific to the IP core which indicate a breakpoint in order to detect the breakpoint.

5. (currently amended) The method of ~~any of~~ claims ~~1 to~~ 4, wherein said switching is performed upon detecting that the breakpoint has been entered.

6. (currently amended) The method of ~~any of~~ claims 1 ~~to 5~~, wherein the IP core is a microprocessor or a DSP.

7. (currently amended) A ~~S~~system for clocking an IP core during a debugging operation, comprising switching means ~~(1)~~;

a clock oscillator or any free-running clock source ~~(2)~~; and

~~-~~control means for sending a control signal to the switching means ~~(1)~~ when the debugging operation

is started, for switching the switching means ~~(1)~~ to the clock oscillator or any free-running clock source ~~(2)~~.